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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/620,472

07/16/2003

David M. Atoji

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9263

(IRA-10-5)

EXAMINER

FRANCIS, MARK P

ART UNIT

PAPER NUMBER

2193

DATE MAILED: 07/17/2006

7590 07/17/2006
DRIGGS LUCAS BRUBAKER & HOGG CO. L.P.A.
DEPT. IRA
8522 EAST AVENUE
MENTOR, OH 44060

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/620,472

Applicant(s)

ATOJI ET AL.

Examiner

Mark P. Francis

Art Unit

2193

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date N/A.

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

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DETAILED ACTION

1. This action is responsive to the application filed on July 16, 2003.
2. Claims 1-19 have been examined.

Oath/Declaration

3. The Office acknowledges receipt of a properly signed oath/declaration filed July 16, 2003.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 1-11 and 19 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Regarding claim 1,

In this instance, the language of the claim raises a question as to whether the claim is directed merely to an abstract idea that is not tied to an environment or machine which would result in a practical application that would produce a useful, concrete, and tangible result to form the basis of statutory subject matter under 35 USC 101.

According to the 101 Interim Guidelines, The tangible requirement does not necessarily mean that a claim must either be tied to a particular machine or apparatus or must operate to change articles or materials to a different state or thing. However, the tangible requirement does require that the claim must recite more than a § 101 judicial

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exception, in that the process claim must set forth a practical application of that § 101 judicial exception to produce a real-world result. Benson, 409 U.S. at 71-72, 175 USPQ at 676-77 (invention ineligible because had "no substantial practical application."). "[An application of a law of nature or mathematical formula to a ... process may well be deserving of patent protection." Diehr, 450 U.S. at 187, 209 USPQ at 8 (emphasis added); see also 21 Corning, 56 U.S. (15 How.) at 268, 14 L.Ed. 683 ("It is for the discovery or invention of some practical method or means of producing a beneficial result or effect, that a patent is granted . . ."). In other words, the opposite meaning of "tangible" is "abstract."

Applicant defines a method for providing a legal sequential combination of commands for verification testing of a computer system. Although Applicant states in the preamble a legal sequential combination of commands for verification testing of a computer system, Applicant has failed to recite, inside the body of the claim the commands actually performing a verification testing function. Applicant merely recites two buckets of commands that contain at least two of the commands arranged in a sequentially ordered sequence legal under at least one rule, and combines the first and second buckets into a sequential bucket test combination. Thus, the claim as a whole and does not produce a tangible, useful, and concrete real-world result, thus failing to result in a practical application.

Regarding claim 19,

Applicant defines a article of manufacture comprising a computer usable medium having a computer readable program embodied in said medium for verification testing of a computer system.

Although Applicant states in the preamble a legal sequential combination of commands for verification testing of a computer system that body of the claim does not support the preamble. Applicant has failed to recite, inside the body of the claim the commands actually performing a verification testing function. Applicant merely recites two buckets of commands that contain at least two of the commands arranged in a sequentially ordered sequence legal under at least one rule, and combines the first and second buckets into a sequential bucket test combination. Thus, the claim as a whole and does not produce a tangible, useful, and concrete real-world result, thus failing to result in a practical application.

The rejection of the base claim are incorporated into their dependent claims.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

7. A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

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8. Claims 1-2, 9-13, and 16-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Parson. (U.S. Pat 6,950,963)

Independent claims

With respect to claims 1,12, and 19, Parson discloses a verification testing system(Col 3:60-67, "...multiple processor test system...") for a computer system, (Col 2:50-67, "...provides a control mechanism for use in testing of integrated circuits and other digital systems which incorporates multiple processors...")comprising: (a) a microprocessor; (Col 3:48-67, "...such as microprocessors...")(b) a central manager connected to the microprocessor and configured to rout command instructions to the microprocessor; (Col 2:50-67, "...The control mechanism then receives one or more commands for each of the processors...software-implemented chain manager...")

(c) a plurality of executable test commands; (Col 3:10-30, "...The test commands...")

(d) at least one rule for forming a legal sequences of commands; (Col 5:20-45, "...to support different sets of semantics for multiple processors, such that commands...")

(e) a first bucket of commands comprising at least two of the executable test commands in a first bucket sequentially ordered sequence legal under the at least one rule; (e.g. See Fig. 1, elements Debug commands for x...for y..." and related text)

and (f) a second bucket of commands comprising at least two of the commands arranged in a second bucket sequentially ordered sequence legal under the at least one

rule; (e.g. See Fig. 1 Chain Manager and JTAG Scan Chain, Fig. 2 Group Scan and related text)

wherein the central manager(Col 4:41-60, "...The chain manager thus delays...") is configured to combine the first bucket and then the second bucket in a sequential bucket test combination having a test sequential order,(Col 4:30-55, "...The individual commands of the groups are then merged...")the sequential bucket test combination having a composite test command sequence legal under the at least one rule, and run the sequential bucket test combination on the microprocessor; (Col 6:56-67, "...a processor by issuing debugger commands to one or more target hardware schedulers...")

and wherein the central manager is further configured to combine the second bucket and then the first bucket into an alternate sequential bucket test combination having an alternate test sequential order,(Col 7:10-35, "...merges JTAG commands from each Tap manager...") the alternate sequential bucket test combination having an alternate composite test command sequence legal under the at least one rule, and run the alternate sequential bucket test combination on the microprocessor. (Col 7:10-60, "...merges JTAG commands from each Tap manager...")

Dependent claims

With respect to claims 2 and 13, the rejection of claims 1 and 12 are incorporated respectively and further, Parson discloses that the executable test commands may be selected from the group comprising arguments of the computer system real operational

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code, specific test instructions targeted for verification purposes, and randomly generated instructions. (Col 3:11-30, "...The test commands for each of the processors...")

With respect to claims 9 and 16, the rejection of claims 1 and 12 are incorporated respectively and further, Parson discloses that the step (r) of assigning a value to the parameter is performed manually discloses that the executable test commands further comprise a parameter for at least one of the plurality of executable commands, and wherein the central manager is configured to assign a value to the parameter. (Col 7:35-60, "...The JTAG chain manager...for a specific non-zero GROUP ID have arrived at the JTAG chain manager...")

With respect to claims 10 and 17, the rejection of claims 9 and 16 are incorporated respectively and further, Parson discloses that the central manager is configured to manually assign a value to the parameter. (Col 7:12-30, "...The chain manager defers issuing a JTAG group scan command...")

With respect to claims 11 and 18, the rejection of claims 9 and 16 are incorporated respectively and further, Parson discloses that the central manager is configured to randomly assign a value to the parameter. (Col 7:12-30, "...The chain manager defers issuing a JTAG group scan command...")

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 3,4,5,6,7,8 and 14,15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parson(U.S. Pat 6,950,963) in view of Duggan.(U.S. Pat 6,002,871)

With respect to claims 3 and 14, the rejection of claims 1 and 12 are incorporated respectively and further,

Parson does not show that the executable test commands further comprise a wait command configured to cause the computer system to pause for at least one instruction cycle, and wherein the step (c) of forming a first bucket of commands further comprises the following step: (i) including said wait command in said first bucket.

Duggan shows that the executable test commands further comprise a wait command configured to cause the computer system to pause for at least one instruction cycle,(Col 14:48-67, "...include a WAIT command...") and wherein the step (c) of forming a first bucket of commands further comprises the following step: (i) including said wait command in said first bucket,(Col 14:48-67, "...include a WAIT command...", Col 19:32-

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45, "...that handles both the WAIT_SSS...") in an analogous system for the purpose of providing enhanced verification of proper execution of the user functions of the application program under test.(Duggan:Col 3:47-50)

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to include a Wait command causing the computer system to pause for one or more instruction cycles.

The modification would have been obvious because one of ordinary skill in the art would have been motivated to send reminder messages to provide enhanced verification of proper execution of the user functions of the application program under test.(Duggan: Col 3:47-50)

With respect to claims 4 and 15, the rejection of claims 1 and 12 are incorporated respectively and further,

Parson does not show that the executable test commands further comprise a wait command configured to cause the computer system to pause for at least one instruction cycle, wherein sequential bucket test combination further comprises said wait command between the first and second buckets, before the first bucket, or after the second bucket.

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Duggan shows that the executable test commands further comprise a wait command configured to cause the computer system to pause for at least one instruction cycle, wherein sequential bucket test combination further comprises said wait command between the first and second buckets, before the first bucket, or after the second bucket. (Col 14:48-67, "...include a WAIT command...", Col 19:32-45, "...that handles both the WAIT_SSS..." in an analogous system for the purpose of providing enhanced verification of proper execution of the user functions of the application program under test.(Duggan:Col 3:47-50)

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to include a Wait command either between the first and second buckets, before the first bucket, or after the second bucket causing the computer system to pause for one or more instruction cycles.

The modification would have been obvious because one of ordinary skill in the art would have been motivated to send reminder messages to provide enhanced verification of proper execution of the user functions of the application program under test.(Duggan: Col 3:47-50)

With respect to claim 5, the rejection of claim 3 is incorporated and further,

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Parson does not show the step (i) of including said wait command in said first bucket further comprises the step of: (m) randomly selecting a point of insertion within the bucket sequentially ordered sequence.

Duggan shows the step (i) of including said wait command in said first bucket further comprises the step of: (m) randomly selecting a point of insertion within the bucket sequentially ordered sequence. (Col 14:48-67, "...include a WAIT command...", Col 19:32-45, "...that handles both the WAIT_SSS...") in an analogous system for the purpose of providing enhanced verification of proper execution of the user functions of the application program under test.(Duggan:Col 3:47-50)

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to randomly select an insertion point within the bucket sequentially order sequence to Parson's invention.

The modification would have been obvious because one of ordinary skill in the art would have been motivated to provide enhanced verification of proper execution of the user functions of the application program under test.(Duggan:Col 3:47-50)

With respect to claim 6, the rejection of claim 4 is incorporated and further,

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Parson does not show the step (j) of including said wait command between the first and second buckets, before the first bucket, or after the second bucket, further comprises the step of: (n) randomly selecting a point of insertion of the wait command within the sequential bucket test combination.

Duggan shows the step (j) of including said wait command between the first and second buckets, before the first bucket, or after the second bucket, further comprises the step of: (n) randomly selecting a point of insertion of the wait command within the sequential bucket test combination.(Col 14:48-67, "...include a WAIT command...", Col 19:32-45, "...that handles both the WAIT_SSS...") in an analogous system for the purpose of providing enhanced verification of proper execution of the user functions of the application program under test.(Duggan:Col 3:47-50)

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to randomly select an insertion point within the bucket test combination to Parson's invention.

The modification would have been obvious because one of ordinary skill in the art would have been motivated to provide enhanced verification of proper execution of the user functions of the application program under test.(Duggan:Col 3:47-50)

With respect to claim 7, the rejection of claim 5 is incorporated and further,

Parson does not show that the step of (i) of including said wait command in said first bucket further comprises the step of (o) inserting a random amount of the wait command.

Duggan shows that the step of (i) of including said wait command in said first bucket further comprises the step of (o) inserting a random amount of the wait command.(Col 14:48-67, "...include a WAIT command...", Col 19:32-45, "...that handles both the WAIT_SSS...") in an analogous system for the purpose of providing enhanced verification of proper execution of the user functions of the application program under test.(Duggan:Col 3:47-50)

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to insert a random amount of the wait command to Parson's invention.

The modification would have been obvious because one of ordinary skill in the art would have been motivated to provide enhanced verification of proper execution of the user functions of the application program under test.(Duggan:Col 3:47-50)

With respect to claim 8, the rejection of claim 6 is incorporated and further,

Parson does not show that the step (j) of including said wait command between the first and second buckets, before the first bucket, or after the second bucket, further comprises the step of (p) inserting a random amount of the wait command.

Duggan shows wherein the step (j) of including said wait command between the first and second buckets, before the first bucket, or after the second bucket, further comprises the step of (p) inserting a random amount of the wait command.(Col 14:48-67, "...include a WAIT command...", Col 19:32-45, "...that handles both the WAIT_SSS...") in an analogous system for the purpose of providing enhanced verification of proper execution of the user functions of the application program under test.(Duggan:Col 3:47-50)

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to insert a random amount of the wait command to Parson's invention.

The modification would have been obvious because one of ordinary skill in the art would have been motivated to provide enhanced verification of proper execution of the user functions of the application program under test.(Duggan:Col 3:47-50)

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

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12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark P. Francis whose telephone number is (571) 272-7956. The examiner can normally be reached on Mon-Fri 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mark P. Francis

Patent Examiner

Art Unit 2193


KAKALI CHAKI
SUPERVISORY PATENT EX-
TECHNOLOGY CENTER

Subst. Form PTO-1449 APPLICANT'S INFORMATION DISCLOSURE STATEMENT	Atty. Docket No.: RPS920010172US1 (IRA-10-5709)		Serial No.: To be assigned
	Applicant: Atoji et al		
	Filing Date: Herewith	Group: To be assigned 2193	

U.S. PATENT DOCUMENTS

Initial*		Document No.	Date	Name	Class	Subcl.	Filing Date
MPF	AA	5,815,688	09/29/1998	Averill	395	500	10/09/1996
MPF	AB	5,646,949	07/08/1997	Bruce, Jr. et al	37	127	06/04/1996
MPF	AC	5,572,666	11/05/1996	Whitman	395	183.08	03/28/1995
MPF	AD	5,488,573	01/30/1996	Brown et al	364	578	09/02/1993
MPF	AE	5,455,938	10/03/1995	Ahmed	364	488	09/14/1994
MPF	AF	5,210,861	05/11/1993	Shimoda	395	575	05/30/1990
MPF	AG	4,984,239	01/08/1991	Suzuki et al	371	3	01/04/1989
	AK						

FOREIGN PATENT DOCUMENTS

		Document No.	Date	Country	Class	Subcl.	Translation?
MPF	AL	JP2001051965A	08/12/1999	Japan	—	—	No
MPF	AM	JP11232131A	02/13/1998	Japan	—	—	No
MPF	AN	JP11230160A	01/16/1998	Japan	—	—	NO
MPF	AO	JP10187475A	12/25/1996	Japan	—	—	No
MPF	AP	JP8166892A	12/13/1994	Japan	—	—	No
MPF	AQ	JP01180645	01/13/1988	Japan	—	—	No

OTHER DOCUMENTS

MPF	AR	"A Biased Random Instruction Generation Environment for Architectural Verification of Pipelined Processors", Journal of Electronic Testing: Theory and Applications, pgs. 13-27 (2000), Ta-Chung Chang
MPF	AS	"Micro Architecture Coverage Directed Generation of Test Programs", Design Automation Conference, June 21-25, 1999, pgs. 175-180
MPF	AT	"Verification by Behavioral Modeling – A Multiprocessor System Case, Conference on ASIC Proceedings", October 21-24, 1996, pgs 43-45
MPF	AU	"Automatic Test Program Generation for Pipelined Processors", IEEE/ACM International Conference on CAD-94, November 6-10, 1994, pgs. 580-583
Examiner: Mark P. Francis		Date Considered: 7/6/06

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if in conformance and not considered.
Include copy of this form with next communication to applicant.

Notice of References Cited	Application/Control No. 10/620,472	Applicant(s)/Patent Under Reexamination ATOJI ET AL.	
	Examiner Mark P. Francis	Art Unit 2193	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,002,871 A	12-1999	Duggan et al.	717/135
*	B	US-6,950,963 B1	09-2005	Parson et al.	714/30
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
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	I	US-			
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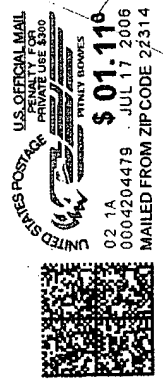
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NON-PATENT DOCUMENTS

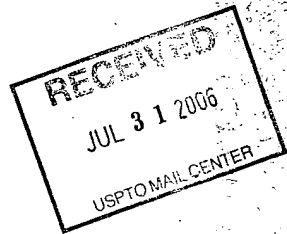
*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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